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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,232	09/17/2003	Hui-Chu Lin	TOPP0009USA	3391

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,232	LIN, HUI-CHU	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 9/17/03. Currently claims 1-13 are pending.

Specification

The disclosure is objected to because of the following informalities: in paragraphs [0017] and [0020], respectively, "offabricating" should read "of fabricating". Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 2 and 3 are objected to because of the following informalities: claims 2 and 3, lines 2 and 3, respectively, the limitation, "further comprising following steps:" should be "further comprising the following steps:".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-10 and 13 rejected under 35 U.S.C. 102(b) as being anticipated by Takemura et al. US Patent 5,719,065.

Takemura discloses the semiconductor method as claimed. See figures 1-11D, and corresponding text with emphasis on figures 9A-9G, pertaining to claim 1, where Takemura teaches a method of fabricating a thin film transistor (TFT) comprising: providing a substrate **101**(figure 9A); forming a polysilicon film **103** on the substrate (col. 5, lines 5-10), the polysilicon film defined with a source region **110**, a drain region **113**, and a channel region between the source region and the drain region (figures 9E and 9F; col. 14, lines 8-21); forming a gate insulating layer **104** on the substrate; forming a gate **105** above the substrate; performing an ion implantation process to form a source in the source region and a drain in the drain region (col. 7, lines 3-6; col. 14, lines 8-27); forming a silicon nitride layer **114** covering the gate and the polysilicon film (col. 14, lines 28-37); and forming a TEOS based silicon oxide layer **115** on the silicon nitride layer (col. 14, lines 46-55).

Pertaining to claim 2, Takemura teaches the method, further comprising the following steps: performing a photo-etching process to form a contact hole on the source and drain respectively; and filling a conductive layer in the contact holes, the conductive layer being electrically connected to the source and the drain (figure 9G; col. 16, lines 7-15).

Pertaining to claim 3, Takemura teaches the method, wherein the method of forming the polysilicon film comprises the following steps: forming an amorphous silicon film on the substrate; and performing an excimer laser annealing process to make the amorphous silicon film crystallize to the polysilicon film (col. 5, lines 5-19; col. 7, lines 40-67, shows laser annealing may be performed by excimer layer).

Pertaining to claim 4, Takemura teaches the method, wherein the silicon nitride layer is a silane based silicon nitride layer. (col. 14, lines 28-37)

Pertaining to claim 6, Takemura teaches the method, wherein the gate is a metal gate (col. 5, lines 45-48).

Pertaining to claim 7, Takemura teaches the method, wherein the silicon oxide has a thickness in a range of 2500 to 10000 angstroms (col. 14, lines 46-47).

Pertaining to claim 8, Takemura teaches the method, wherein the silicon nitride has a thickness in a range of 500 to 3500 angstroms (col. 14, lines 35-36).

Pertaining to claim 9, Takemura teaches the method, wherein the silicon nitride layer is formed by performing a first plasma enhanced chemical vapor deposition (PECVD) process (col. 14, lines 28-36; ***Note***: it is inherent that plasma CVD is another terminology for PECVD. See *Stanley Wolf and Richard N. Tauber Vol. I, Second Edition, Silicon Processing For The VLSI Era, page 176, under Plasma Enhanced CVD: Physics, Chemistry, & Reactor Designs*).

Pertaining to claim 10, Takemura teaches the method, wherein the silicon oxide layer is formed by performing a second plasma enhanced chemical vapor deposition process (col. 14, lines 46-48; ***Note***: it is inherent that plasma CVD is another terminology for PECVD. See *Stanley Wolf and Richard N. Tauber Vol. I, Second Edition, Silicon Processing For The VLSI Era, page 176, under Plasma Enhanced CVD: Physics, Chemistry, & Reactor Designs*).

Pertaining to claim 13, Takemura teaches the method, wherein the low temperature polysilicon thin film transistor is a top gate low temperature polysilicon thin film transistor or a bottom gate low temperature polysilicon thin film transistor (figure 9G, top gate TFT).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 11, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura et al. US Patent 5,719,065 in view of *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Volume I, Second Edition, pages 170-180 and 202-206, Copyright 2000.*

Takemura discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1-4, 6-10, and 13, under 35 U.S.C. 102(b). In addition, Takamura teaches, pertaining to claim 5, the method of claim 4, wherein the silicon nitride layer serves as a hydrogen source of a hydrogenating process (col. 14, lines 37-45).

However, Takemura fails to show, pertaining to claim 5, the method of claim 4, wherein the silicon nitride layer comprises 20% to 40% hydrogen atoms. Takemura also fails to show, pertaining to claim 11, the method wherein the first PECVD process and the second PECVD process are performed in the same chamber. Finally, Takemura fails to show, pertaining to claim 12, the method wherein the first PECVD process and the second PECVD process are performed in different chambers.

Wolf teaches on pages 178-179, two different types of PECVD reactors, used for conventional PECVD processing, that will include the method wherein the first PECVD process and the second PECVD process are performed in the same chamber and, the method wherein the first PECVD process and the second PECVD process are performed in different chambers. Wolf also teaches on pages 202-206, a silicon nitride film formed by conventional chemical vapor deposition techniques.

It would have been obvious to one of ordinary skill in the art to have incorporated, the silicon nitride layer comprising 20% to 40% hydrogen atoms, in the method of Takemura, pertaining to claim 5, according to the combined teachings of Takemura and Wolf, with the motivation that, both methods are performed under conventional techniques. In particular, Takemura teaches a conventional silicon nitride film 114, wherein an annealing process is performed after the silicon nitride film is deposited, and the hydrogen contained in the silicon nitride film, is diffused to improve the defects existing to the surface of the silicon oxide film 104 and source/drain regions 110 and 113. Wolf teaches on pages 202-206, a conventional silicon nitride film, formed by PECVD, is made of 10%-30% atomic hydrogen. Therefore, the claimed silicon nitride layer comprising 20% to 40% hydrogen atoms is considered to be within conventional specifications, especially since no criticality has been shown.

It would have been obvious to one of ordinary skill in the art to have incorporated, the method wherein the first PECVD process and the second PECVD process are performed in the same chamber or, the method wherein the first PECVD process and the second PECVD process are performed in different chambers, in the method of Takemura, pertaining to claims 11 and 12, according to the teachings of Wolf, with the motivation that, as stated in Wolf, pages 178-179, the Mini-Batch Radical Cold-Wall Reactor, called the Concept One®, when operated as a PECVD reactor, can be used to deposit sequentially several different types of dielectric films, resulting in the confirmation that the first and second PECVD processes can be formed within the same chamber. On the other hand, Wolf teaches that the multi-chamber single wafer system, called the Precision 5000®, connects different types of reactor chambers, which can be programmed to execute paralleled identical processes, wherein each CVD chamber contains a

gas dispersion, resulting in the confirmation, that the first PECVD process and the second PECVD process may be performed in different chambers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
August 23, 2004

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